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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,622	12/21/2001	Abbas Rashid	NEXSI-01224US0	7941

28863 7590 07/22/2005

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ART UNIT	**PAPER NUMBER**
2666	

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,622	RASHID ET AL.	
	Examiner	Art Unit	
	Puneet Bhandari	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-76* is/are rejected.

7)☒ Claim(s) *77-79* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08). Paper No(s)/Mail Date *04/22/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims **39-42,46,47,51-54 & 58-62** are objected to because of the following informalities:

Regarding claim **39**, an objection is made to the use of phrase "adapted to" on line 4. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **40**, an objection is made to the use of phrase "adapted to" on line 2 & line 4. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **41**, an objection is made to the use of phrase "adapted to" on line 2 & line 4. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **42**, an objection is made to the use of phrase "adapted to" on line 1. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **46**, an objection is made to the use of phrase "adapted to" on line 5, line 6, line 9 & line 12. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **47**, an objection is made to the use of phrase "adapted to" on line 2 & line 4. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **51**, an objection is made to the use of phrase "adapted to" on line 5. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **52**, an objection is made to the use of phrase "adapted to" on line 2 & line 4. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **53**, an objection is made to the use of phrase "adapted to" on line 2, and line 4. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **54**, an objection is made to the use of phrase "adapted to" on line 1 .The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **58**, an objection is made to the use of phrase "adapted to" on line 5. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **59**, an objection is made to the use of phrase "adapted to" on line 5. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **60**, an objection is made to the use of phrase "adapted to" on line 3 and line 6. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **61**, an objection is made to the use of phrase "adapted to" on line 3 and line 6. The use of this phrase is an optional language (see MPEP-2106.II.C).

Regarding claim **62**, an objection is made to the use of phrase "adapted to" on line 1. The use of this phrase is an optional language (see MPEP-2106.II.C).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim **50** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 50 recites the limitation "said storage buffer" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims **39** is rejected under 35 U.S.C. 102(e) as being anticipated by Dai et al. (US 6,658016).

Regarding claim **39**, an apparatus is anticipated by Fig. 3 with a plurality of inputs (Input port-88 A_0", A_1" A_2" .....A_7"), a FIFO storage buffer (330), a requesting logic (packet buffer control unit-340) coupling plurality of inputs (Input port-88 A_0", A_1" A_2" .....A_7") to said FIFO storage buffer (330) also disclosed in column 13, lines 30-60.

The limitation a memory (memory unit) in communication with the said requesting logic (packet buffer control unit-340), said memory concurrently maintain a plurality of pointers; each pointer in said plurality of pointers corresponds to a different location in said storage buffer for storing data from an input port in said set of input ports is anticipated by the packet buffer control unit includes a memory unit for storing pointer address location information associated with each of the received data packets disclosed in column 14, lines 1-10.

7. Claim **39-66, 71 & 72** are rejected under 35 U.S.C. 102(e) as being anticipated by Mann et al. (US 6,212,165).

Regarding claim **39**, an apparatus is anticipated by element 10 of fig 3 with plurality of input (ports 12), a FIFO storage buffer (input and output queues), request logic (port combiner) coupling said plurality of inputs to said FIFO storage buffer (input and output queues are FIFO queues) also disclosed in column 4, lines 13-65.

The limitation, memory (RAM column 5, lines 31-39) in communication with said request logic (port combiner) is anticipated by port combiner is connected input and output RAM as disclosed in Fig 3.

The limitation memory concurrently maintains plurality of pointers is anticipated by read and write pointers disclosed in column 5, lines 38-54. The reference discloses RAM maintaining read and write pointers.

The limitation, each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports is anticipated by fig. 4 also refer column 5, lines 38-54.

Regarding claims **40, 52 & 60,** the limitation said memory includes a first entry to maintain a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from the input port in said set of input port is anticipated by write pointer_1 corresponding to the first location to store the data from the ports column 5, lines 38-54 also refer fig 4.

The limitation, said memory includes a second entry to maintain a pointer corresponding to a second location in said FIFO storage buffer (input queue) for storing

a first set of data from the input port in said set of input port is anticipated by write pointer_2 corresponding to the second location to store the data from the ports column 5, lines 38-54 also refer to fig 4.

Regarding claim **41, 47, 53 & 61,** the limitation, said memory includes a third entry to maintain a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from the input port in said set of input port is anticipated by write pointer_3 corresponding to the third location to store the data from the ports column 5, lines 38-54 also refer fig 4.

The limitation, said memory includes a fourth entry to maintain a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from the input port in said set of input port is anticipated by the write pointer_N corresponding to the fourth location to store the data from the ports column 5, lines 38-54 also refer fig 4.

Regarding claim **42, 54 & 62** the limitation, the memory maintain a data identifier (data segment) for each pointer in said plurality of pointers is anticipated by pointers for segments as disclosed in column 5, lines 30-39.

Regarding claim **43, 55 & 63,** the limitation, data identifier identifies a data source (attributes) is anticipated by data segment contains frame data and the associated attributes disclosed in column 5, lines 30-39.

Regarding claim **44, 48, 56 & 64,** the limitation, said memory is a content addressable memory is anticipated by RAM disclosed in column 4, lines 44-54.

Regarding claim **45, 49, 57 & 65,** the limitation, said request logic (port combiner) and said storage buffer (input queue-36) are included in multiple port memory (Multiple input /output FIFO queue-10) is anticipated by Fig 3.

Regarding claim **46**, an apparatus is anticipated by element 10 of Fig. 3 with plurality of input (ports 12), a FIFO storage buffer (input and output queues), request logic (port combiner) coupling said plurality of inputs to said FIFO storage buffer (input and output queues are FIFO queues) also disclosed in column 4, lines 13-65.

The limitation, memory (RAM column 5, lines 31-39) in communication with said request logic (port combiner) is anticipated by Fig. 3. The reference discloses port combiner is connected input and output RAM.

The limitation, memory (RAM column 5, lines 31-39) concurrently maintains plurality of pointers is anticipated by read and write pointers disclosed in column 5, lines 38-54. The reference discloses RAM maintaining read and write pointers.

The limitation, each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports is anticipated by Fig 4 and also refer in column 5, lines 38-54.

The limitation, said memory includes a first entry to maintain a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from the input port in said set of input port is anticipated by write pointer_1 corresponds to the first location to store the data from the ports column 5, lines 38-54 also refer fig 4.

The limitation said memory includes a second entry to maintain a pointer corresponding to a second location in said FIFO storage buffer (input queue) for storing

a first set of data from the input port in said set of input port is anticipated by write pointer_2 corresponds to the second location to store the data from the ports column 5, lines 38-54 also refer fig 4.

Regarding claim **50**, the limitation, a sink port comprising a plurality of data inputs (inputs port 12 to port combiner-30), a multiple entry FIFO (10) having a plurality of inputs in communication with said plurality of data inputs to accept and store data is anticipated by Fig 3.

The limitation, an output port (external ports) coupled to said multiple entry FIFO (10) to receive said data from a storage buffer (40) and transmit the data on a communication link (resources) is anticipated by Fig 3 and also disclosed in column 1, lines 63-67 and column 2, lines 1-10. The reference discloses multiple entry FIFO could use where several external ports share same resources (communication link).

Regarding claim **51 & 59**, the limitation a FIFO storage buffer (input and output queues), request logic (port combiner) coupling said plurality of inputs to said FIFO storage buffer (input and output queues are FIFO queues) is anticipated by Fig 3 and also disclosed in column 4, lines 13-65.

The limitation, memory (RAM column 5, lines 31-39) in communication with said request logic (port combiner) is anticipated by Fig. 3. The reference discloses port combiner is connected input and output RAM.

The limitation memory (RAM column 5, lines 31-39) concurrently maintains plurality of pointers is anticipated by read and write pointers disclosed in column 5, lines 38-54. The reference discloses RAM maintaining read and write pointers

The limitation each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports is anticipated by Fig 4 and also disclosed in column 5, lines 38-54.

Regarding claim **58**, the limitation, a cross-bar switch comprising of a set of input ports (12) to receive data packets, a set of sink port (10) in communication with said set of input ports to accept and forward said data packets is anticipated by Fig 3 and also disclosed in column 6, lines 9-23

The limitation, a multiple entry FIFO (10) having a plurality of data inputs to store data packets accepted by the said first sink port is anticipated by Fig 2 and disclosed in column 6, lines 9-23.

Regarding claim **66**, the limitation, wherein each sink port (10) in said set of sink ports includes a multiple entry point FIFO is anticipated by Fig 2.

Regarding claim **71**, a method for a sink port (10) in a cross-bar switch to collect data in a FIFO, is anticipated by Fig.2 said method comprising the steps of

(a) The step of accepting data from a first data packet, wherein said data accepted in aid set (a) is a subset of said first data packet is anticipated by Fig 2.The reference discloses receiving the data from the ports (12).

(b) The step of storing the data from the first data packet in a said FIFO is anticipated by Fig 2. The reference discloses storing the data in multiple input/single output FIFO queue.

(c) The step of accepting data from a second data packet, wherein said data accepted in aid step (c) is a subset of said second data packet is anticipated by anticipated by Fig 2.The reference discloses receiving the data from the second port.

(d) The step of storing said data from said second data packet in said FIFO is anticipated by anticipated by Fig 2.The reference discloses storing the data in multiple input/single output FIFO queue.

Regarding claim **72**, the limitation said first packet originates from a first source (port 12) and said second packet originated from a second sources (port 12) is anticipated by Fig. 2 disclosed in column 4, lines 53-65.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim **67-70 & 73-76** rejected under 35 U.S.C. 103(a) as being unpatentable over Mann et al. (US 6,212,165) in further view of Dai et al.

Regarding claim **67**, Mann et al. teaches all the limitations of claim 67 (see the 102 rejection for claim 58 above). Mann et al fails to disclose a set of data rings in communication with said set of input ports and said set of sink ports. Fig 2 of Dai et al discloses a set of data rings (data ring and control ring) in communication with set of input port (Input port-88 A_0", A_1" A_2" .....A_7") and output ports (output port-88 A_0', A_1', A_2'.....A_7').At the time invention was made, it would have been obvious to a person in

ordinary skill in art to use Dai et al. data rings to connect sink input ports and input ports of Mann et al. One in ordinary skill in art would have been motivated to do so since ring architecture switching fabric allows higher frequencies and greater throughput between devices (see column 2, lines 1-7 of Dai et al.).

Regarding claim **68**, Mann et al. teaches all the limitations of claim 68 (see the 102 rejection for claim 58 above) and Fig 2. Mann et al. also discloses multiple entry point FIFO that includes a data input for each port. Mann et al fails to disclose a set of data rings in communication with multiple entry point FIFO. Fig 2 of Dai et al discloses a set of data rings (data ring and control ring) in communication with set of input port (Input port-88 A_0", A_1" A_2" .....A_7") and output ports (output port-88 A_0', A_1', A_2'.....A_7').At the time invention was made, it would have been obvious to a person in ordinary skill in art to modify the multiple entry point FIFO of Mann et al. to include data input for each data ring in said set of data rings of Dai et al. One in ordinary skill in art would have been motivated to do so since ring architecture switching fabric allows higher frequencies and greater throughput between devices (see column 2, lines 1-7 of Dai et al.).

Regarding claim **69**, Mann et al. teaches all the limitations of claim 69 (see the 102 rejection for claim 58 above). Mann et al. fails to disclose first sink port snoops data packets on each data ring in said set of data ring and determines whether to accept said first data packet based on set criteria, said first sink port having sufficient storage space for storing said first data packet and said first sink port supporting a destination targeted by said first data packet.

Dai et al discloses, the limitation said first sink port snoops data packets on each data ring in said set of data ring and determines whether to accept said first data packet based on set criteria is anticipated by destination managing unit coupled to the sink port determine whether to accept data packet, disclosed in column 12, lines 63-67 and column 15, lines 1-29; wherein said set of criteria includes,

The step of said first sink port having sufficient storage space for storing said first data packet is anticipated by output buffer manager monitors the availability of buffer space in corresponding one of transmit buffer queues disclosed in column 15, lines 45-55,

The step said first sink port supporting a destination targeted by said first data packet is anticipated by packet routing and control unit which is coupled to the sink port reads the destination address of the data packet disclosed in column 14, lines 11-36, and

The step a total number of packets being received by said first sink port not exceeding a predetermined number of packets is anticipated by destination managing unit monitor the data packet so that the amount of packet received by the sink port does not exceed a threshold amount of buffer space as disclosed in column 10, lines 29-36 and column 29 lines 65-66 and column 30, lines 1-67.

At the time invention was made, it would have been obvious to a person in ordinary skill in art to add Dai et al. method wherein first sink port snoops data packets on each data ring in said set of data ring and determines whether to accept said first data packet based on set criteria, said first sink port having sufficient storage space for storing said

first data packet and said first sink port supporting a destination targeted by said first data packet sink ports and input ports of Mann et al. One in ordinary skill in art would have been motivated to provide a switching fabric allows higher frequencies and greater throughput for transferring data between devices (see column 2, lines 1-7 of Dai et al.).

Regarding claim **70**, Mann et al. teaches all the limitations of claim 69 (see the 102 rejection for claim 58 above) and Fig 2 of Mann et al. discloses a sink port (10) with multiple entry point FIFO (multiple input/ single output FIFO) and Fig 3 output port (40) coupled to said multiple point entry FIFO to receive data from multiple point entry FIFO and transmit the data on a communication link (transmitting the data to switching fabric on a communication link). Mann et al. fails to disclose a sink port with a ring interface to couple to said set of data rings and plurality of outputs on a ring interface to receive and store said data from the said ring interface. Dai et al discloses in Fig 3A said sink port (output ports-84 A_0', A_1', A_2'.....A_7') includes a ring interface (interface 248 to couple data ring to the sink port) coupled to said set of data rings to receive data from data packets also disclosed in column 12, lines 40-63.At the time invention was made, it would have been obvious to a person in ordinary skill in art to modify the multiple entry point FIFO of Mann et al. to include data input for each data ring in said set of data rings of Dai et al. One in ordinary skill in art would have been motivated to do so since ring architecture switching fabric allows higher frequencies and greater throughput between devices (see column 2, lines 1-7 of Dai et al.).

Regarding claim **73**, Mann et al. discloses all the limitation of claim 73 but Mann et al. fails to disclose (e) determining that said data accepted in said step (a) includes a

first line of said first data packet; (f) allocating a first location in said FIFO for storing data from said first data packet; (g) determining that said data accepted in said step (c) includes a first line of said second data packet and (h) allocating a second location in said FIFO for storing data from said second data packet. Dai et al. discloses switching fabric that perform (e) the step of determining that said data accepted in said step (a) includes a first line of said first data packet is anticipated by reading the header information of the packet disclosed in column 14, lines 1-35; (f) allocating a first location in said FIFO for storing data from said first data packet is anticipated by pointer reg-1 disclosed in column 18, lines 35-53; (g) determining that said data accepted in said step (c) includes a first line of said second data packet is anticipated by reading the header information of the packet disclosed in column 14, lines 1-10;and (h) allocating a second location in said FIFO for storing data from said second data packet is anticipated by pointer reg-2 disclosed in column 18, lines 35-53. At the time invention was made it would have been obvious to one in ordinary skill in art to combine Multiple Input/ Single output sink port of Mann et al with the switching fabric of Dai et al. one in ordinary skill in art would have been motivated to do so to provide a switching fabric allows higher frequencies and greater throughput for transferring data between devices (see column 2, lines 1-7 of Dai et al.).

Regarding claim **74**, Mann et al. further fails to teach step (f) includes the steps of (1) creating a pointer to said first location (2) creating a first tag identifying said first data packet. Dai et al. discloses switching fabric that perform (1) creating a pointer to said first location is anticipated by pointer reg-1 disclosed in column 18, lines 35-53 and (2)

creating a first tag identifying said first data packet is anticipated by using the header information to route the data packet disclosed in column 14, lines 11-35. At the time invention was made it would have been obvious to one in ordinary skill in art to combine Multiple Input/ Single output sink port of Mann et al with the switching fabric of Dai et al. one in ordinary skill in art would have been motivated to do so to provide a switching fabric allows higher frequencies and greater throughput for transferring data between devices (see column 2, lines 1-7 of Dai et al.).

Regarding claim **75**, Mann et al. further fails to teach step (h) includes the steps of (1) creating a pointer to said second location (2) creating a second tag identifying said second data packet. Dai et al. discloses switching fabric that perform (1) creating a pointer to said first location is anticipated by pointer reg-2 disclosed in column 18, lines 35-53 and (2) creating a second tag identifying said first data packet is anticipated by using the header information to route the data packet disclosed in column 14, lines 11-35. At the time invention was made it would have been obvious to one in ordinary skill in art to combine Multiple Input/ Single output sink port of Mann et al with the switching fabric of Dai et al. one in ordinary skill in art would have been motivated to do so to provide a switching fabric allows higher frequencies and greater throughput for transferring data between devices (see column 2, lines 1-7 of Dai et al.).

Regarding claim **76**, Mann et al. further fails to teach wherein first tag identifies a source of first data packet and second tag identifies a source of said second data packet. Dai et al. discloses each data packet (first and second data packet) includes a header that specifies source of each data packet as disclosed in column 14, lines 10-35.

At the time invention was made it would have been obvious to one in ordinary skill in art to combine Multiple Input/ Single output sink port of Mann et al with the switching fabric of Dai et al. one in ordinary skill in art would have been motivated to do so to provide a switching fabric allows higher frequencies and greater throughput for transferring data between devices (see column 2, lines 1-7 of Dai et al.).

Allowable Subject Matter

10. Claims **77-79** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cao (US 6,700,899), Niu (6,625,157), Yu et al. (6,725,270), Caldara et al. (US 5,978,359), Akella et al. (US 6,697,362) and Wong et al. (US 6,614,758).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Puneet Bhandari whose telephone number is 571-272-2057. The examiner can normally be reached on 9.00 AM To 5.30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Puneet Bhandari
Examiner
Art Unit 2666

PB
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Seema S. Rao 7/19/05
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